REMARKS

Claims 1-45 are pending in the present application. Applicants respectfully request reconsideration of the present application in view of the remarks presented herein.

RESTRICTION

In the Office Action mailed June 12, 2007, in the above captioned case, the Examiner has stated that the present Application contains six distinct inventions. As such, the Examiner has required the Applicants to elect a single invention for prosecution on the merits.

Specifically, the Examiner has required the Applicants to elect between a first invention, Group I, recited in claims 1-8 [sic], classified in class 717, subclass 131, ("data processing: software development, installation, and management, software program development tool [e.g., integrated case tool or stand-alone development tool], testing or debugging including analysis of program execution") drawn to:

fetching from memory a first machine language instruction comprising an instruction segment;

responsive to a trigger pattern in said first machine language instruction, modifying said instruction segment to form a second machine language instruction; and

executing on said processor said second machine language instruction,

and a second invention, Group II, recited in claims 8 [sic] -16, classified in class 712, subclass 248 ("processing architecture: writable/changeable control store architecture") , drawn to:

fetching from memory a first machine language instruction comprising an instruction segment;

responsive to a trigger pattern in said first machine language instruction, accessing instruction modification information from a memory;

modifying said instruction segment according to said instruction modification information and information associated with said trigger pattern to form a second machine language instruction; and

executing on said processor said second machine language instruction,

and a third invention, Group III, recited in claims 17-22, classified in class 712, subclass 25 ("processing architecture: data driven or demand driven processor"), drawn to:

A computer system comprising:

a memory for storing a first machine language instruction;

a processor coupled to said memory for executing machine language instructions;

said processor also for implementing a method, said method comprising:

fetching from said memory said first machine language instruction comprising an instruction segment from said memory;

responsive to a trigger pattern in said first machine language instruction, modifying said instruction segment to form a second machine language instruction; and

executing on said processor said second machine language instruction,

and a fourth invention, Group IV, recited in claims 23-32, classified in class 717, subclass 143 ("data processing: software development, installation, and management, compiling code, analysis of code form, parsing, syntax analysis, and semantic analysis"), drawn to:

a memory stored packet contained within a very long instruction word, said packet comprising

a trigger pattern to initiate modification of a segment of said very long instruction word;

a first field to indicate a portion of said segment to be modified; and

a second field to indicate how to modify said portion of said segment,

and a fifth invention, Group V, recited in claims 33-36, classified in class 711, subclass 215 ("electrical computers: memory, address formation in response to microinstruction") drawn to:

accessing said machine language instruction from memory;

recognizing a trigger pattern in said machine language instruction;

identifying a portion of said machine language instruction; and

modifying said portion of said machine language instruction to form a second machine language instruction,

and a sixth invention, Group VI, recited in claims 37-45, classified in class 710, subclass 54 ("electrical computers: input/output, queue content modification"), drawn to:

accessing from memory an instruction word comprising a plurality of instruction segments and a trigger portion;

based on said trigger portion, identifying a portion of information of a memory queue for selection thereof;

based on said trigger portion, identifying a portion of one of said plurality of instruction segments;

modifying said portion of said one of said plurality of instruction segments with said portion of information of said memory queue; and

dispatching said one of said plurality of instruction segments, as modified by said modifying, to an execution unit of said processor.

It is appreciated that the Examiner has quoted each recited independent claim, and alleges a classification unique to each entire recited independent claim.

ELECTION WITH TRAVERSE BETWEEN

GROUPS I, II, III, IV, V AND VI

In order to be responsive, Applicants provisionally elect, with traverse, the invention of Group I, recited in claims 1-8 [sic], classified in class 717, subclass 131, drawn to:

fetching from memory a first machine language instruction comprising an instruction segment;

responsive to a trigger pattern in said first machine language instruction, modifying said instruction segment to form a second machine language instruction; and

executing on said processor said second machine language instruction.

Arguments in Traverse

MPEP § 803 explains that restriction is only proper if "[t]here would be a serious burden on the examiner if restriction is not required (see MPEP § 803.02, § 808, and § 808.02)." Applicants note that all recited claims were previously examined, in rejections dated 6/26/06 and 12/20/06. Such history of previous examination appears to infer that the examination is not seriously burdensome, and that therefore the required "serious burden" is not present.

For this reason, Applicants respectfully assert that the present six-way restriction requirement is improper, and respectfully solicit withdrawal of the restriction requirement.

"If the search and examination of all the claims in an application can be made without serious burden, the examiner must examine them on the merits, even though they include claims to independent or distinct inventions" (MPEP § 803, emphasis added).

As the previous examination has established that examination of all claims of the present application is not a "serious burden," Applicants respectfully assert that the MPEP directs the Examiner to examine all claims of

the present application on the merits. For this additional reason, Applicants respectfully assert that the present restriction requirement is improper, and respectfully solicit withdrawal of the restriction requirement.

Moreover, the previous rejections dated 6/26/06 and 12/20/06 contained at least one single rejection against claims from all of the newly alleged independent inventions. For example, Claims 1-5 (newly alleged Group I), 8, 9-14 (newly alleged Group II), 17, 18, 20 (newly alleged Group III), 23 (newly alleged Group IV) and 34-36 (newly alleged Group V) and 37 (newly alleged Group VI) were rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by Nunomura (US 6,871,274, "Nunomura").

Applicants respectfully assert that the previous rejection of claims representing all of the newly alleged inventions over a single piece of art under 35 U.S.C. § 102 adds further weight against a serious examination burden. In addition, the previous rejection over a single reference under 35 U.S.C. § 102 appears to argue against the newly alleged multiple classifications.

As the history of examination fails to support the newly alleged multiple classifications, Applicants respectfully assert that the present six-way restriction requirement is improper. For this further reason, Applicants respectfully solicit withdrawal of the restriction requirement.

In addition to the previous arguments in traverse of the restriction requirement, Applicants respectfully traverse at least the following classifications.

The Examiner alleges Group I, recited in claims 1-8 [sic], as classified in class 717, subclass 131. This class is defined as "data processing: software development, installation, and management, software program development tool [e.g., integrated case tool or stand-alone development tool], testing or debugging including analysis of program execution."

Applicants traverse this classification. Claim 1, allegedly part of Group I, recites:

> A method of executing a processor instruction, said method comprising:
>
> fetching from memory a first machine language instruction comprising an instruction segment;
>
> responsive to a trigger pattern in said first machine language instruction, modifying said instruction segment to form a second machine language instruction; and
>
> executing on said processor said second machine language instruction.

Applicants respectfully assert that the claimed limitations of Claim 1 are not directed to "software development," or "software program development tools," or "testing or debugging" or "analysis of program execution" as required by class 717, subclass 131.

For these reasons, Applicants respectfully assert that the classification of the alleged Group I invention is incorrect, and respectfully solicit correction of the classification. Moreover, as the classification of the alleged Group I invention is incorrect, Applicants respectfully assert that the basis for restriction is correspondingly incorrect. For this reason, Applicants respectfully solicit withdrawal of the restriction requirement.

The Examiner alleges Group III, recited in claims 17-22, as classified in class 712, subclass 25. This class is defined as "processing architecture: data driven or demand driven processor."

Applicants traverse this classification. Claim 17, allegedly part of Group III, recites:

A computer system comprising:

a memory for storing a first machine language instruction;

a processor coupled to said memory for executing machine language instructions;

said processor also for implementing a method, said method comprising: (the method recited in Claim 1).

Applicants respectfully assert that the claimed limitations of Claim 17 are not directed to a data driven or demand driven processor, as those terms are understood by those of ordinary skill in the art, and as they are used in the USPTO classification schedule for class 712, subclass 25.

For these reasons, Applicants respectfully assert that the classification of the alleged Group III invention is incorrect, and respectfully solicit correction of the classification. Moreover, as the classification of the alleged Group III invention is incorrect, Applicants respectfully assert that the basis for restriction is correspondingly incorrect. For this reason, Applicants respectfully solicit withdrawal of the restriction requirement.

Further with respect to alleged Group III, the alleged invention of Group III recites a processor for implementing the method recited in Claim 1 (Group I). Applicants fail to understand how a processor for implementing a method of a first group can attain status as an allegedly different group, under a separate classification.

For this further reason, Applicants respectfully solicit withdrawal of the restriction requirement.

The rejection argues that inventions I and III are separately usable, as invention I "which does not have the processor coupled to the memory for executing machine language instructions (as in Group III). Applicants respectfully traverse. Group I recites "executing on said processor said second machine language instruction." Thus, an apparatus for implementing the method of Group I must have a processor capable of executing machine language instructions, in contrast to the rejection's allegation. Further, Group III recites all the limitation of independent Claim 1 (Group I).

For this still further reason, Applicants respectfully solicit withdrawal of the restriction requirement.

The Examiner alleges Group IV, recited in claims 23-32, classified in class 717, subclass 143. This class is defined as "data processing: software development, installation, and management, compiling code, analysis of code form, parsing, syntax analysis, and semantic analysis."

Applicants traverse this classification. Claim 23, allegedly part of Group IV, recites:

a memory stored packet contained within a very long instruction word, said packet comprising

a trigger pattern to initiate modification of a segment of said very long instruction word;

a first field to indicate a portion of said segment to be modified; and

a second field to indicate how to modify said portion of said segment.

Applicants respectfully assert that the claimed limitations of Claim 23 are not directed to "software development," or "compiling code," or "analysis of code form" or "parsing" or "syntax analysis" or "semantic analysis" as required by class 717, subclass 143.

For these reasons, Applicants respectfully assert that the classification of the alleged Group IV invention is incorrect, and respectfully solicit correction of the classification. Moreover, as the classification of the alleged Group IV invention is incorrect, Applicants respectfully assert that the basis for restriction is correspondingly incorrect. For this reason, Applicants respectfully solicit withdrawal of the restriction requirement.

CONCLUSION

Claims 1-45 are pending in the present application. Applicants respectfully request reconsideration of the present application in view of the remarks presented herein.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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Date: 7/12/2007

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